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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,422	09/16/2003	Hiroshi Sumihiro	7217/70905	2711

7590 12/15/2005  
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EXAMINER

STIGLIC, RYAN M

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/663,422		SUMIHIRO, HIROSHI	
	<b>Examiner</b>		<b>Art Unit</b>	
	Ryan M. Stiglic		2112	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. Claims 1-3 are pending and have been examined.
2. Claims 1-3 are rejected.

### ***Response to Arguments***

3. Applicant's arguments filed September 26, 2005 have been fully considered but they are not persuasive. With respect to applicant's arguments relating to Kurth, Hewitt, and Nunziata being silent of "the feature of the present invention wherein the priority determination means determines priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder and the second result judging whether or not the request signals received from other modules based on the first result..." the Examiner respectfully disagrees. The Examiner respectfully submits that every request priority determination circuit works in this manner. In general, a priority determination circuit (means) first detects a request from a device (first result of the newly added limitation). Second, if a request is detected from said device the request competes in an arbitration sequence with requests from other requesting devices (second result of the newly added limitation). Third, a winning request is granted access to the system resource based on priority determination criteria. As clearly seen by the Examiner's brief explanation of priority determination systems, applicant's newly added limitation reads directly on a standard priority determination system.
4. As stated below in section 8, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder. Furthermore, an encoder and decoder are required components of modules of an information processing apparatus, as they are

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responsible for properly formatting data into appropriate configurations. In other words encoders and decoders are responsible for properly formatting (encoding) data into a format compliant with a transmission protocol and further responsible for formatting (decoding) data received from a transmission media into a format compliant with an individual module. For the remainder of the Office Action the encoder and decoder of claims 1-3 will be considered required and inherent features of every module of the information processing system.

5. The new declaration filed September 26, 2005 has been accepted.

### *Drawings*

6. The drawings were received on September 28, 2005. These drawings are acceptable.

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With regards to claim 1, it is unclear as to whether an encoder and a decoder are a part of the receiving means, a part of the plurality of modules, or an example of modules. Likewise, claim 3 is unclear as to whether the encoder and decoder are examples of modules or are components of the modules. For the sake of advancing prosecution the Examiner will

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interpret an encoder and decoder to be part of each module of the information processing apparatus.

9. Claims 1-3 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With regards to claim 1, it is unclear to which “step of determining priority” claim 1 is referring to since claim 1 is drawn to an apparatus (not a method) including priority determination means (not a step of determining priority). Likewise in claim 3, it is unclear to which “priority determination means” claim 3 is referring to since claim 3 is drawn to a method (not an apparatus) and includes the step of determining priority.

*Claim Rejections - 35 USC § 102*

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurth (6880028B2).

For claim 1:

An information processing apparatus comprising:

- receiving means having a plurality of inputs for respectively receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, req lines are received by Arbiter 102 through a plurality of receiving means; col. 2, ll. 65-66) including an encoder and a decoder (As stated above in section 4, the Examiner

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understands each module of the information processing apparatus to include an encoder and a decoder) ;

- measurement means for measuring time limit of each of said plurality of modules based on the request signal received by each of said plurality of inputs of said receiving means (Fig. 2, 202; col. 3, ll. 25-26; col. 5, ll. 17-27; Fig. 6);
- priority determination means for determining a priority of bus acquisition of said plurality of modules according to the time limit measured by said measurement means (Fig. 6; col. 5, ll. 17-27); and
- control means for controlling acquisition of the bus for said plurality of modules based on the priority determined by said priority determination means (col. 3, ll. 1-17);
- wherein said step of determining priority determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 2, ll. 65-67) and the second result judging whether or not the request signals received from other modules based on the first result (col. 3, ll. 1-17).

For claim 2:

The information processing apparatus according to claim 1, wherein said priority determination means determines priority by means of a round-robin method when there is a plurality of modules having a same time limit as measured by said measurement means (col. 3, ll. 1-17).

For claim 3:

An information processing method comprising the steps of:

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- receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, req lines are received by Arbiter **102** through a plurality of receiving means; col. 2, ll. 65-66) including an encoder and a decoder (As stated above in section 4, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder);
- measuring time limit of each of said plurality of modules based on a request signal requesting bus acquisition received for each of the plurality of modules (Fig. 2, 202; col. 3, ll. 25-26; col. 5, ll. 17-27; Fig. 6);
- determining priority of bus acquisition of said plurality of modules according to a time limit as measured in said of measuring (Fig. 6; col. 5, ll. 17-27); and
- controlling acquisition of bus for said plurality of modules based on the priority as determined in said step of determining priority (col. 3, ll. 1-17);
- wherein said priority determination means determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 2, ll. 65-67) and the second result judging whether or not the request signals received from other modules based on the first result (col. 3, ll. 1-17).

12. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Nunziata et al. (5572686).

For claim 1:

An information processing apparatus comprising:

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- receiving means having a plurality of inputs for respectively receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, 22; col. 3, ll. 31-33) including an encoder and a decoder (As stated above in section 4, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder);
- measurement means for measuring time limit of each of said plurality of modules based on the request signal received by each of said plurality of inputs of said receiving means (col. 4, ll. 61-64);
- priority determination means for determining a priority of bus acquisition of said plurality of modules according to the time limit measured by said measurement means (col. 3, ll. 19-37; col. 4, line 35 – col. 5, line 10); and
- control means for controlling acquisition of the bus for said plurality of modules based on the priority determined by said priority determination means (col. 3, ll. 27-29);
- wherein said step of determining priority determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 3, ll. 31-33) and the second result judging whether or not the request signals received from other modules based on the first result (col. 3, ll. 27-31).

For claim 2:

The information processing apparatus according to claim 1, wherein said priority determination means determines priority by means of a round-robin method when there is a plurality of modules having a same time limit as measured by said measurement means (col. 7, ll. 25-28).

For claim 3:

An information processing method comprising the steps of:

- receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, 22; col. 3, ll. 31-33) including an encoder and a decoder (As stated above in section 4, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder);
- measuring time limit of each of said plurality of modules based on a request signal requesting bus acquisition received for each of the plurality of modules (col. 4, ll. 61-64);
- determining priority of bus acquisition of said plurality of modules according to a time limit as measured in said of measuring (col. 3, ll. 19-37; col. 4, line 35 – col. 5, line 10);  
and
- controlling acquisition of bus for said plurality of modules based on the priority as determined in said step of determining priority (col. 3, ll. 27-29).
- wherein said priority determination means determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 2, ll. 31-33) and the second result judging whether or not the request signals received from other modules based on the first result (col. 3, ll. 27-31).

13. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Hewitt et al. (5956493).

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For claim 1:

An information processing apparatus comprising:

- receiving means having a plurality of inputs for respectively receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, 180 & REQ[7:0]; col. 3, line 61 – col. 4, line 10) including an encoder and a decoder (As stated above in section 4, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder);
- measurement means for measuring time limit of each of said plurality of modules based on the request signal received by each of said plurality of inputs of said receiving means (col. 4, ll. 31-44);
- priority determination means for determining a priority of bus acquisition of said plurality of modules according to the time limit measured by said measurement means (col. 4, ll. 11-22); and
- control means for controlling acquisition of the bus for said plurality of modules based on the priority determined by said priority determination means (col. 3, line 61 – col. 4, line 10)
- wherein said step of determining priority determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 3, line 61 – col. 4, line 10) and the second result judging whether or not the request signals received from other modules based on the first result (col. 4, ll. 11-22; col. 4, ll. 54-57).

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For claim 3:

An information processing method comprising the steps of:

- receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, 180 & REQ[7:0]; col. 3, line 61 – col. 4, line 10) including an encoder and a decoder (As stated above in section 4, the Examiner understands each module of the information processing apparatus to include an encoder and a decoder);
- measuring time limit of each of said plurality of modules based on a request signal requesting bus acquisition received for each of the plurality of modules (col. 4, ll. 31-44);
- determining priority of bus acquisition of said plurality of modules according to a time limit as measured in said of measuring (col. 4, ll. 11-22); and
- controlling acquisition of bus for said plurality of modules based on the priority as determined in said step of determining priority (col. 3, line 61 – col. 4, line 10);
- wherein said priority determination means determines said priority of the bus acquisition by the first result judging whether or not the request signal is received from the encoder or the decoder (col. 3, line 61 – col. 4, line 10) and the second result judging whether or not the request signals received from other modules based on the first result (col. 4, ll. 11-22; col. 4, ll. 54-57).

### *Claim Rejections - 35 USC § 103*

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hewitt et al as applied to claim 1 above and what was well known in the art as evidenced by Tran (5519837).

As stated above Hewitt teaches receiving means having a plurality of inputs for respectively receiving a request signal for requesting bus acquisition for each of a plurality of modules (Fig. 1, 180 & REQ[7:0]; col. 3, line 61 – col. 4, line 10); measurement means for measuring time limit of each of said plurality of modules based on the request signal received by each of said plurality of inputs of said receiving means (col. 4, ll. 31-44); priority determination means for determining a priority of bus acquisition of said plurality of modules according to the time limit measured by said measurement means (col. 4, ll. 11-22); and control means for controlling acquisition of the bus for said plurality of modules based on the priority determined by said priority determination means (col. 3, line 61 – col. 4, line 10). *Official Notice* is taken in that implementing round robin selection methods are well known arbitration methods in the art. Round Robin arbitration algorithms are useful for resolving conflicting requests from devices of equal priority because they ensure fairness while providing good throughput, as evidenced by Tran (col. 1, ll. 30-37).

### ***Conclusion***

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

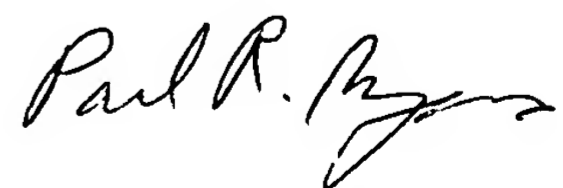
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS



PAUL R. MYERS  
PRIMARY EXAMINER